

Vu H. N. Phan

Curriculum Vitae

Portland, Oregon
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vuphan314
vuphan314



Vu Phan is a Formal Verification engineer at Intel Corporation; he performs pre-Silicon validation of Intellectual Properties. Vu earned a Ph.D. degree in Computer Science at Rice University; his advisor was Prof. Moshe Vardi.

Experience

- 2022-now **IP Verification Engineer**, *Intel Corporation*, Full-time, Hybrid (Portland, Oregon).
 - Perform pre-Silicon Formal Verification of Intellectual Properties in Systems on ChipsSkills: Computer Architecture, SystemVerilog, TCL
- 2017-2022 **Graduate Research Assistant**, *Rice University*, Full-time, On-site (Houston, Texas).
 - Designed and implemented algorithms to solve stochastic satisfiability with Prof. Moshe VardiSkills: C++, Python
- 2021 **IP Verification Engineer**, *Intel Corporation*, Internship, Remote (Dallas, Texas).
 - Developed software to benchmark Formal Property Verification platforms

Certifications

- 2025/01 **Jasper Formal Expert v22.09**, *Cadence Design Systems*.
- 2023/03 **Jasper Formal Fundamentals v21.09**, *Cadence Design Systems*.
- 2021/07 **SVA, Formal, and JasperGold Fundamentals for Designers v19.03**, *Cadence Design Systems*.

Education

- 2020-2022 **Doctor of Philosophy in Computer Science**, *Rice University*, GPA 3.63/4.00.
- 2017-2019 **Master of Science in Computer Science**, *Rice University*, GPA 3.60/4.00.
- 2014-2017 **Bachelor of Science in Computer Science & Math**, *Texas Tech University*, GPA 4.00/4.00.
- 2013-2014 **Associate of Science**, *Collin College*, GPA 4.00/4.00.

Projects

- 2019-2021 **DPMC**, *Dynamic-Programming Model Counter*, <https://github.com/vardigroup/DPMC>.
 - Implemented a weighted-#SAT framework with Jeffrey Dudek
- 2018-2019 **ADDMC**, *Algebraic-Decision-Diagram Model Counter*, <https://github.com/vardigroup/ADDMC>.
 - Implemented a weighted-#SAT solver
- 2016-2018 **LED**, *Language of Effective Definitions*, <https://vuphan314.github.io/LED>.
 - Translated the literate-programming language LED into SequenceL and LaTeX
- 2015-2016 **L**, *Logic*, <https://github.com/iensen/LtoASPtranslator>.
 - Translated the logic-programming language L into Answer Set Prolog with Evgenii Balai

Computing Courses

2017-2021 Graduate Level.

1. Reasoning about Software
2. Bioinformatics: Sequence Analysis
3. Statistical Machine Learning
4. Computer Systems Architecture
5. Multi-Core Computing
6. Compiler Construction
7. Artificial Intelligence
8. Programming Languages
9. Automated Program Verification
10. Logic in Computer Science

2015-2017 Undergraduate Level.

1. Operating Systems
2. Database Systems
3. Computer Architecture
4. Programming Languages
5. Software Engineering
6. Algorithms
7. Object-Oriented Programming
8. Computer Organization and Assembly Language
9. Modern Digital System Design
10. Data Structures
11. Automata
12. Programming Principles

Bibliography

Vu Phan is the correspondence author of the following publications (authors are sorted by surnames).

Theses

- [Pha22] Vu H. N. Phan. “Quantitative Reasoning on Hybrid Formulas with Dynamic Programming”. PhD thesis. Rice University, 2022. URL: <https://repository.rice.edu/items/2e464125-244d-431b-b998-612f0dc2b41a>.
- [Pha19] Vu H. N. Phan. “Weighted Model Counting with Algebraic Decision Diagrams”. MS thesis. Rice University, 2019. URL: <https://repository.rice.edu/items/a1a5e73d-a001-44ca-9730-25a7277c8af1>.

Conference Papers

- [DPV21] Jeffrey M. Dudek, Vu H. N. Phan, and Moshe Y. Vardi. “ProCount: Weighted Projected Model Counting with Graded Project-Join Trees”. In: *Conference on Theory and Applications of Satisfiability Testing (SAT)*. 2021. URL: https://kasekopf.github.io/papers/sat21_procount.pdf.
- [DPV20a] Jeffrey M. Dudek, Vu H. N. Phan, and Moshe Y. Vardi. “DPMC: Weighted Model Counting by Dynamic Programming on Project-Join Trees”. In: *Conference on Principles and Practice of Constraint Programming (CP)*. 2020. URL: <https://arxiv.org/abs/2008.08748>.
- [DPV20b] Jeffrey M. Dudek, Vu H. N. Phan, and Moshe Y. Vardi. “ADDMC: Weighted Model Counting with Algebraic Decision Diagrams”. In: *AAAI Conference on Artificial Intelligence (AAAI)*. 2020. URL: <https://arxiv.org/abs/1907.05000>.

Workshop Paper

- [Pha18] Vu H. N. Phan. “Syntactic Conditions for Antichain Property in Consistency Restoring Prolog”. In: *Workshop on Answer Set Programming and Other Computing Paradigms (ASPOCP)*. 2018. URL: <https://arxiv.org/abs/1809.09319>.