2025/08/06

Vu H. N. Phan

Resume

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- Vu Phan validated semiconductor *Intellectual Property (IP)* as a *Formal Verification (FV)* engineer at Intel Corporation. He earned a PhD in Computer Science under Prof. Moshe Vardi's supervision at Rice University.
- Vu is a permanent resident of the United States. He is fluent in English and Vietnamese, as well as in programming languages for hardware (SystemVerilog), software (C++), data analysis (Python), and technical writing (LaTeX).

Work Experience

End 2025/07 Start 2022/10 **IP FV Engineer**, Intel Corporation (Oregon).
- Performed pre-Silicon *Formal Property Verification (FPV)* of System-on-Chip hardware
- Co-owned the Cache-Coherence Fabric, which orchestrates communication among CPU cores
  - Error-Correcting Codes in Last-Level Cache: Reliability, Availability, Serviceability
  - Machine-Check Architecture: error types; overwriting rules
  - Power Management: request-acknowledgment handshakes; Finite State Machines
- Used SystemVerilog to develop FPV references and Python to analyze bounds of assertions

End 2021/08 Start 2021/05 **IP FV Engineering Intern**, Intel Corporation (Texas).
- Developed software to benchmark FPV platforms

End 2022/08 Start 2017/08 **Graduate Research Assistant**, Rice University (Texas).
- Designed and implemented algorithms to solve stochastic satisfiability with Prof. Moshe Vardi
- Used C++ to develop solvers, Python to analyze datasets, and LaTeX to typeset documents

Higher Education

End 2022/08 Start 2020/01 **Doctor of Philosophy in Computer Science**, Rice University.
- Published conference papers [DPV20a; DPV21] and thesis [Pha22]

End 2019/12 Start 2017/08 **Master of Science in Computer Science**, Rice University.
- Published conference paper [DPV20b] and thesis [Pha19]

End 2017/07 Start 2014/08 **Dual Bachelor of Science in Computer Science and Math**, Texas Tech University.
- Published workshop paper [Pha18]

Software Development

End 2022 Start 2020 **DPMC**, *Dynamic-Programming Model Counter*, `https://github.com/vardigroup/DPMC`.
- Implemented a weighted-#SAT framework with Jeffrey Dudek

End 2019 Start 2018 **ADDMC**, *Algebraic-Decision-Diagram Model Counter*, `https://github.com/vardigroup/ADDMC`.
- Implemented a weighted-#SAT solver
- Won the weighted track of the Model Counting Competition 2020 (tied with another solver)

End 2017 Start 2016 **LED**, *Language of Effective Definitions*, `https://vuphan314.github.io/LED`.
- Implemented a translator from the literate-programming language LED to SequenceL and LaTeX

End 2016 Start 2015 **L**, *Logic*, `https://github.com/iensen/LtoASPtranslator`.
- Implemented a translator from the logic-programming language L to Answer Set Prolog with Evgenii Balai
- Invented CertWare Safety Case Workbench with five other innovators (NASA NTR: LAR-18868-1)

Computing Coursework

End 2022 **Graduate Level**.

Start 2017

1. Statistical Machine Learning
2. Artificial Intelligence
3. Reasoning about Software
4. Bioinformatics: Sequence Analysis
5. Multi-Core Computing
6. Compiler Construction

End 2017 **Undergraduate Level**.

Start 2015

1. Data Structures
2. Object-Oriented Programming
3. Database Systems
4. Operating Systems
5. Computer Organization and Assembly Language
6. Modern Digital System Design

Bibliography

Vu Phan is the corresponding author of the following publications (authors are sorted by surnames).

Theses

[Pha22] Vu H. N. Phan. "Quantitative Reasoning on Hybrid Formulas with Dynamic Programming". PhD thesis. Rice University, 2022. URL: https://repository.rice.edu/items/2e464125-244d-431b-b998-612f0dc2b41a.

[Pha19] Vu H. N. Phan. "Weighted Model Counting with Algebraic Decision Diagrams". MS thesis. Rice University, 2019. URL: https://repository.rice.edu/items/a1a5e73d-a001-44ca-9730-25a7277c8af1.

Conference Papers

[DPV21] Jeffrey M. Dudek, Vu H. N. Phan, and Moshe Y. Vardi. "ProCount: Weighted Projected Model Counting with Graded Project-Join Trees". In: *Conference on Theory and Applications of Satisfiability Testing (SAT)*. 2021. URL: https://kasekopf.github.io/papers/sat21_procount.pdf.

[DPV20a] Jeffrey M. Dudek, Vu H. N. Phan, and Moshe Y. Vardi. "DPMC: Weighted Model Counting by Dynamic Programming on Project-Join Trees". In: *Conference on Principles and Practice of Constraint Programming (CP)*. 2020. URL: https://arxiv.org/abs/2008.08748.

[DPV20b] Jeffrey M. Dudek, Vu H. N. Phan, and Moshe Y. Vardi. "ADDMC: Weighted Model Counting with Algebraic Decision Diagrams". In: *AAAI Conference on Artificial Intelligence (AAAI)*. 2020. URL: https://arxiv.org/abs/1907.05000.

Workshop Paper

[Pha18] Vu H. N. Phan. "Syntactic Conditions for Antichain Property in Consistency Restoring Prolog". In: *Workshop on Answer Set Programming and Other Computing Paradigms (ASPOCP)*. 2018. URL: https://arxiv.org/abs/1809.09319.